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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,160	12/04/2001	Takashi Yamada	50090-459	8255

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EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,160	YAMADA, TAKASHI	
	Examiner	Art Unit	
	David Ton	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. Claims 1-6 are presented for examination.

Claim Rejections - 35 USC ' 112

3. Claim 1 is rejected under 35 U.S.C. ' 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 1, it is not clear to the Examiner that how many semiconductor devices are there under test? In the preamble, on line 1, Applicant claimed "a method of testing a semiconductor storage device" which means testing a singular of semiconductor storage device. On the other hand, on lines 4, 6 and 8 of the claim, Applicant claimed "semiconductor storage devices" which means testing a plurality of semiconductor storage devices.

Claim Rejections - 35 USC ' 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Sugamori patent no. 6,314,034, in view of Kawaguchi patent no. 4,628,509.

6. As to claim 1, Sugamori teaches the invention substantially as claimed, including a method of testing a semiconductor storage device [memory DUT 19 of Fig. 7A], comprising the steps of:

Setting a plurality of test patterns [see ALPG, col. 5 line 66 – col. 6 line 6] in a tester for testing semiconductor storage devices [see claim 1];

Applying different test patterns to respective semiconductor storage devices connected to said tester [inherently, see claim 2 and col. 6 lines 28-35 "test for different devices or different blocks in the device in parallel at the same time"]; and

Sugamori teaches determining a repair algorithm for executing a memory repair process in the memory; however, Sugamori does not teach determining whether or not results of the tested semiconductor storage devices fall within a predetermined tolerance.

Kawaguchi teaches a testing apparatus for redundant memory by an analysis of the remedy judgment whether the memory to be "NG" (no good) and subsequent failure results are not input for it or the testing is continued to the end for those of the memories for which the analysis indicates the possibility of

remedy, even if failure data has been input for them [see col. 3 lines36-55]. Another word, Kawaguchi teaches determining whether or not results of the tested redundant memory fall within a predetermined tolerance [the number of failures in the same column or row lines do not exceeds the number of redundant lines prepared along the other side, see col. 4 lines 25-37].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the teachings of Sugamori to provide a test system including an analysis of the remedy judgment as taught by Kawaguchi. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would providing a memory tester which can conduct data analysis at high speed [see Kawaguchi, col. 2 lines 50-57].

7. As to claim 2, Kawaguchi teaches the number of defective bit lines having exceed a tolerance is compared with the number of redundant lines on the basis of test result output, thereby determining semiconductor storage devices which can be restored through use of redundant lines [col. 4 lines 25-37].

8. As to claim 3, Kawaguchi teaches the number of defective column lines having exceed a tolerance is compared with the number of redundant lines on the basis of test result output, thereby determining semiconductor storage devices which can be restored through use of redundant lines [col. 4 lines 25-37].

9. Claims 4 and 6 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Sugamori patent no. 6,314,034, in view of Kawaguchi patent no. 4,628,509 and further in view of White, Jr. et al. (White) patent no. 4,642,784.

10. As to claim 4, Sugamori and Kawaguchi do not teach a test is performed several times while a test pattern is changed.

White teaches a method of semiconductor memory device test including applying an electrical test sequence to the memory device, said sequence including a first selected pattern of data and a second selected pattern of data [see claim 12].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the teachings of Sugamori and Kawaguchi to include performing a test several times while a test pattern is changed as taught by White. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would providing a memory tester which can apply to a manufacture semiconductor testing.

11. As to claim 6, White teaches a test pattern is made by combination of a voltage, a time, and a signal [see Fig. 2 and col. 1 lines 20-22].

12. Claim 5 is rejected under 35 U.S.C. § 103 (a) as being unpatentable over Sugamori patent no. 6,314,034, in view of Kawaguchi patent no. 4,628,509 and further in view of Watanabe patent no. 5,724,289.

13. AS to claim 5, Sugamori and Kawaguchi do not teach testing a non-volatile memory including writing and erasure tests.

Watanabe teaches testing a non-volatile memory including writing and erasure tests [see claim 2].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the teachings of Sugamori and Kawaguchi to include writing and erasure tests for a non-volatile memory as taught by Watanabe. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would providing a memory tester which can apply to a non-volatile memory testing.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

DT

March 02, 2004

DAVID TON
PRIMARY EXAMINER